PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10083411	02/27/2002	716	13	2825	DO

**APPLICANTS: Stenberg Robert; Pavisic Ivan;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed ☐ yes ☑ no		ATTORNEY DOCKET NO
35 USC 119 conditions met ☐ yes ☑ no		
Verified and Acknowledged Examiners's intials TD		01-926 72242 (6653)

TITLE : System and method for identifying and eliminating bottlenecks in integrated circuit designs

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	THUAN -DO Assistant Examiner	CLAIMS ALLOWED	
		Total Claims 18	Print Claim for O.G 1
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. 4 / Figs.Drwg. 7 / Print Fig. 2	
☐ TERMINAL DISCLAMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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